



UNITED STATES PATENT AND TRADEMARK OFFICE

UNITED STATES DEPARTMENT OF COMMERCE
United States Patent and Trademark Office
Address: COMMISSIONER FOR PATENTS
P.O. Box 1450
Alexandria, Virginia 22313-1450
www.uspto.gov

APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
09/733,402	12/08/2000	Stephen R. Vogel	DIVA /203	1879

56015 7590 10/07/2005

MOSER, PATTERSON & SHERIDAN, LLP/
SEDNA PATENT SERVICES, LLC
595 SHREWSBURY AVENUE
SUITE 100
SHREWSBURY, NJ 07702

EXAMINER

RAMPURIA, SATISH

ART UNIT	PAPER NUMBER
----------	--------------

2191

DATE MAILED: 10/07/2005

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No. 09/733,402	Applicant(s) VOGEL ET AL.	
	Examiner Satish S. Rampuria	Art Unit 2191	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

- 1) ☒ Responsive to communication(s) filed on 12 July 2005.
- 2a) ☒ This action is **FINAL**. 2b) ☐ This action is non-final.
- 3) ☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

- 4) ☒ Claim(s) 27-35 and 48-56 is/are pending in the application.
- 4a) Of the above claim(s) _____ is/are withdrawn from consideration.
- 5) ☐ Claim(s) _____ is/are allowed.
- 6) ☒ Claim(s) 27-35 and 48-56 is/are rejected.
- 7) ☐ Claim(s) _____ is/are objected to.
- 8) ☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

- 9) ☐ The specification is objected to by the Examiner.
- 10) ☐ The drawing(s) filed on _____ is/are: a) ☐ accepted or b) ☐ objected to by the Examiner.
Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).
Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).
- 11) ☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

- 12) ☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).
- a) ☐ All b) ☐ Some * c) ☐ None of:
1. ☐ Certified copies of the priority documents have been received.
 2. ☐ Certified copies of the priority documents have been received in Application No. _____.
 3. ☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).
- * See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

- | | |
|--|---|
| 1) <input type="checkbox"/> Notice of References Cited (PTO-892) | 4) <input type="checkbox"/> Interview Summary (PTO-413)
Paper No(s)/Mail Date. _____ |
| 2) <input type="checkbox"/> Notice of Draftsperson's Patent Drawing Review (PTO-948) | 5) <input type="checkbox"/> Notice of Informal Patent Application (PTO-152) |
| 3) <input type="checkbox"/> Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08)
Paper No(s)/Mail Date _____ | 6) <input type="checkbox"/> Other: _____ |

10

DETAILED ACTION

1. This action is in response to the Amendment filed on July 12, 2005.
2. The rejection under 35 U.S.C. §101 to claims 27-35 is withdrawn in view of applicant's amendment and Remarks.
3. Claims are previously cancelled by the Applicant: 1-26 and 36-47.
4. New claims added by the Applicant: 55-56.
5. Claims are pending: 27-35 and 48-56

Response to Arguments

6. Applicant's arguments with respect to claims have been considered but they are not persuasive.

In the remarks, the applicant has argued that:

- (i) The combination of Herrmann, Tang, and Sasaki fails to teach or suggest "transferring said second file to a server comprising a processor board coupled to a plurality of functional elements, each said functional element comprising a programmable logic device coupled to a switching circuit," in the combination with the enabling the switching circuit corresponding to each programmable logic device having said identified target files via said first bus" as recited in independent claim 27.

Examiner's response:

- (i) In response to Applicants argument regarding the limitation "transferring said second file to a server comprising a processor board coupled to a plurality of functional elements, each said functional element comprising a programmable

Art Unit: 2191

logic device coupled to a switching circuit,” in the combination with the enabling the switching circuit corresponding to each programmable logic device having said identified target files via said first bus.” All three references are directed towards the programming PLD. Herrmann system does provide an apparatus and method for programming of integrated circuits containing programmable elements (see the abstract). Sasaki system provides a method and apparatus to program PLDs (see the abstract). Tang system provide remotely programming a PLD (see the abstract). The limitation “transferring said second file to a server comprising a processor board coupled to a plurality of functional elements, each said functional element comprising a programmable logic device coupled to a switching circuit,” in the combination with the enabling the switching circuit corresponding to each programmable logic device having said identified target files via said first bus” is taught by Hermann in combination with Tang and Sasaki. It is noted that the rejection clearly points out where Herrmann, Tang and Sasaki teach the claimed features and why it would have been obvious to combine their teachings. Rather, in response to applicant's arguments against the references individually, one cannot show nonobviousness by attacking references individually where the rejections are based on combinations of references. See *In re Keller*, 642 F.2d 413, 208 USPQ 871 (CCPA 1981); *In re Merck & Co.*, 800 F.2d 1091, 231 USPQ 375 (Fed. Cir. 1986). Further, as indicated by the Applicant that claims 52, 30 and 51 are directly or indirectly dependent on claims 48 and 27 have the these limitations as described above. However,

Art Unit: 2191

these limitations are recited in the independent claims 27 and 48 only and are taught by the combination of Hermann Tang and Sasaki as explained above.

Therefore, the rejection is proper and maintained herein.

7. **THIS ACTION IS MADE FINAL.** Applicant is reminded of the extension of time policy as set forth in 37 CFR 1.136(a).

A shortened statutory period for reply to this final action is set to expire **THREE MONTHS** from the mailing date of this action. In the event a first reply is filed within **TWO MONTHS** of the mailing date of this final action and the advisory action is not mailed until after the end of the **THREE-MONTH** shortened statutory period, then the shortened statutory period will expire on the date the advisory action is mailed, and any extension fee pursuant to 37 CFR 1.136(a) will be calculated from the mailing date of the advisory action. In no event, however, will the statutory period for reply expire later than **SIX MONTHS** from the mailing date of this final action.

Claim Rejections - 35 USC § 103

8. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

(a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negated by the manner in which the invention was made.

9. Claims 27-29, 31-35, 48-50 and 53-56 are rejected under 35 U.S.C. 103(a) as being unpatentable over Herrmann et al., hereinafter called Herrmann, US Patent No.

Art Unit: 2191

6,134,707 and further in view of Tang, US Patent No. 6,389,321 and further in view of Sasaki, hereinafter called Sasaki, US Patent No. 6,198,304.

As per claims 27 and 34 Herrmann discloses:

- *programming a first file in a non-native format for programming said one or more programmable logic devices from a remote programmer source* (Abstract, “a device configuration program with adaptive programming source code instructions (non-native format) that characterize device (programmable) configuration instructions and data”);
- *converting said non-native format programmable logic instructions into a second file having programmable logic instructions in a format native to said remote programmable logic device* (Abstract, “An interpreter converts the device configuration program into formatted device (programmable) configuration instructions and data”). It is interpreted that file is being converted it must be stored in a format which processor understand, and processor is included inherently.
- *programming said identified programmable logic devices via a second bus coupled to said switching circuit* (col. 4, lines 56-60 “The PCB... includes... embedded controller 34... JTAG interface circuitry... A bus... route... programming signals... to the IC” and col. 6, lines 36-38 “The ISP controller then shifts the control and programming data serially into the target ISP device via SDI/TDI”).

Herrmann does not explicitly disclose transferring said second file to a server comprising a processor board coupled to a plurality of functional elements each said functional element comprising a programmable logic device coupled to a switching

Art Unit: 2191

circuit; executing the converted file for identifying particular target files associated with said programmable logic devices via a first bus coupled to switching circuits.

However, Tang disclose in an analogous computer system *transferring said second file to a server* (col. 1, lines 42-43 “sending and receiving data (file) over a communication link” and col. 3, lines 4-5 “programming data 107 can be provided by an ispSTREAMfile”) *comprising a processor board coupled to a plurality of functional elements* (col. 2, lines 63-66 “a programming device... coupled by a wired data network... to remote ISP systems”), *each said functional element comprising a programmable logic device coupled to a switching circuit* (col. 1, lines 44-45 “Each ISP system include one or more ISP controllers for programming multiple ISP devices”), *executing the converted file* (col. 5, lines 61-65 “The microprocessor, which executes a program stored in the non-volatile memory), *for identifying particular target files associated with said programmable logic devices* (col. 6, lines 27-28 “The ISP controller then reads an identification code (ID) from each ISP device in the daisy-chain” and col. 6, lines 33-35 “The ISP controller compares the ID... ISP device with the ID specified in the programming data, to ensure that the correct ISP device is programmed”), *via a first bus coupled to switching circuits* (col. 4, lines 49-50 “The programming data stored in RAM 607 can be provided to ISP controller 402 via data bus”).

Therefore, it would have been obvious to a person of ordinary skill in the art at the time the invention was made to program PLD via communication medium, execute file, and program PLD via a bus as taught by Tang in corresponding to program PLD as taught by Herrmann. The modification would be obvious because of one of ordinary

Art Unit: 2191

skill in the art would be motivated to program PLD remotely including execution and programming a PLD as suggested by Tang (col. 1, lines, 25-33).

Neither Herrmann nor Tang system discloses enabling the switching circuit corresponding to each programmable logic device having said identifiers target files via said first bus.

However, Sasaki disclose in an analogous computer system enabling the switching circuit corresponding to each programmable logic device having said identifiers target files via said first bus (col. 13, lines 56-57 “This orders the programming circuit to switch from examining the thirty-two bit data streams to examining data streams as eight bit sequences” col. 21 lines 51-54 “switching circuit selectively chooses which of said two arrays are addressed in response to signals at said input node” also figs. 6-9 and related discussion). It would be obvious to enable switching circuits to a PLD.

Therefore, it would have been obvious to a person of ordinary skill in the art at the time the invention was made to include switching circuit to program PLD as taught by Sasaki in corresponding to the program PLD as taught in the combination system by Herrmann and Tang. The modification would be obvious because of one of ordinary skill in the art would be motivated to include switching circuit to control the data in the system to program PLD (col. 1, lines 17-27).

As per claim 28, the rejection of claim 27 is incorporated and further Herrmann discloses:

Art Unit: 2191

- *wherein said first file is a programmer object file (POF)* (col. 2, lines 22-24 “a programming object file (POF) is loaded onto the computer running the programming software”).

As per claim 29, the rejection of claim 27 is incorporated, and further Herrmann does not explicitly disclose wherein said remote programmer source is selected from the group comprising a workstation, and a personal computer.

However, Tang discloses in an analogous computer system *wherein said remote programmer source is selected from the group comprising a workstation, and a personal computer* (col. 2, lines 10-13 “Each host computer includes a central processing unit, which may be a personal computer or an engineering workstation, and an access interface for accessing the communication link”).

The feature of selecting a programming source would be obvious for the reasons set forth in the rejection of claim 27.

As per claim 31 the rejection of claim 27 is incorporated, and further Herrmann does not explicitly disclose *wherein said communications medium is an Ethernet network*.

However, Tang discloses in an analogous computer system *wherein said communications medium is an Ethernet network* (col. 2, lines 13-15 “host units... coupled by a computer network... a local area network or a wide area network”).

The feature of communications medium is an Ethernet network would be obvious for the reasons set forth in the rejection of claim 27.

Art Unit: 2191

As per claim 32 the rejection of claim 27 is incorporated, and further Herrmann disclose:

- *wherein said native format comprises a JTAG format* (Abstract, “formatted device configuration instructions and data are preferably compatible with IEEE 1149.1 JTAG-BST specifications”).

As per claim 33, the rejection of claim 27 is incorporated, and further Herrmann does not explicitly disclose *wherein said first bus is a board select bus*.

However, Tang discloses in an analogous computer system *wherein said first bus is a board select bus* (col. 5, lines 12-16 “The data processing... include... sub-system functional components: a processor 64, memory 66, input/output circuitry 68, and peripheral devices 70. These components are coupled together by a system bus 72”).

The feature of bus is a board select bus would be obvious for the reasons set forth in the rejection of claim 27.

As per claim 35 the rejection of claim 27 is incorporated and further it is interpreted that after programming is done the device must enter in initial operating state to function properly and to make the new changes in effect.

Claims 48 and 54 are the apparatus claim corresponding to method claim 27 and rejected under the same rational set forth in connection with the rejection of claim 27 above.

As per claim 49, the rejection of claim 48 is incorporated and further Herrmann discloses:

Art Unit: 2191

- *wherein said first and second bus is a backplane* (col. 4, lines 49-56 “The programming data stored... provided... via data bus...under... microprocessor ... provides a control signal... for latching... data into ISP controller 402. In this manner, the multiple ISP controllers in ISP system 600 can program a large number of ISP devices in parallel, without incurring large latencies due to the long daisy-chains of ISP devices”).

Claim 50 is the apparatus claim corresponding to method claim 32 and rejected under the same rational set forth in connection with the rejection of claim 32 above.

As per claim 53, the rejection of claim 48 is incorporated and further Tang discloses:

- *wherein processor system is a server* (col. 2, lines 59-61 “the ISP system is programmed by remote access by a host programming system which includes one or more programming host computers”).

Per claim 55:

The rejection of claim 27 is incorporated, and further, Herrmann disclose:

- wherein said executing step is via a parallel bus. It would be obvious to execute using the parallel bus because the circuit board is connected via a parallel bus.

Per claim 56:

The rejection of claim 27 is incorporated, and further, Herrmann disclose:

Art Unit: 2191

- wherein said programming step is via a serial bus (col. 2, lines 30-32 “downloaded from the computer to the board containing the PLD via a serial cable that is compliant with the JTAG-BST interface, causing the PLD to be programmed”).

10. Claim 52 is rejected under 35 U.S.C. 103(a) as being unpatentable over Herrmann, Tang, Sasaki and further in view of admitted prior art.

As per claim 52, the rejection of claim 48 is incorporated, and further, neither Herrmann nor Tang nor Sasaki disclose wherein said at least one programmable logic device is selected from the group comprising a gate array, field programmable gate array, programmable, field programmable logic array, read only memory, programmed array logic, programmable logic array, and complex programmable logic devices.

However, admitted prior art discloses in an analogous computer system wherein said at least one programmable logic device is selected from the group comprising a gate array, field programmable gate array, programmable, field programmable logic array, read only memory, programmed array logic, programmable logic array, and complex programmable logic devices (Applicant’s specification, page 1, lines 12-13 “programmable logic devices (PLDs), such as field programmable gate array (FPGAs and the like, are well known”).

Therefore, it would have been obvious to a person of ordinary skill in the art at the time the invention was made to incorporate the selecting of devices is selected from the group comprising gate array as taught in admitted prior art in corresponding to programming PLD as taught in combination system by Herrmann, Tang, and Sasaki.

Art Unit: 2191

The modification would be obvious because of one of ordinary skill in the art would be motivated to select from the group of device to program as PLD as suggested in admitted prior art (Applicant's specification, page 4, lines 1-4).

11. Claims 30 and 51 are rejected under 35 U.S.C. 103(a) as being unpatentable over Herrmann, Tang, Sasaki in view of technical paper from Altera Corporation published in May 1999, ver. 6, hereinafter called Altera Corporation.

As per claim 30 the rejection of claims 27 is incorporated and neither Herrmann nor Tang nor Sasaki explicitly disclose using a JAM byte code file.

However, Altera Corporation discloses in an analogous computer system using the JAM byte code file the time of programming PLD (page 7, paragraph 1 "The Jam language allow a sing Jam file (.jam) or Jam Byte-Code file (.jbc) to contain both the data to be programmed into a device and the algorithm required to accomplish programming).

Therefore, it would have been obvious to a person of ordinary skill in the art at the time the invention was made to include the JAM byte code file to program PLDs as taught by Altera Corporation in the programming and remotely programming PLDs as taught by Herrmann and Tang. The modification would be obvious because of one of ordinary skill in the art would be motivated to include the JAM byte code file to reduce the time, file size and large algorithms in system programming as suggested by Altera Corporation (page 6, paragraph 3 "The Jam™ programming... in-system programming").

Claim 51 is the apparatus claim corresponding to method claim 30 and rejected under the same rational set forth in connection with the rejection of claim 30 above.

Art Unit: 2191


Conclusion

12. Any inquiry concerning this communication or earlier communications from the examiner should be directed to **Satish S. Rampuria** whose telephone number is **(571) 272-3732**. The examiner can normally be reached on **8:30 am to 5:00 pm** Monday to Friday except every other Friday and federal holidays.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, **Tuan Q. Dam** can be reached on **(571) 272-3695**. The fax phone number for the organization where this application or proceeding is assigned is 703-872-9306.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see <http://pair-direct.uspto.gov>. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

Satish S. Rampuria
Patent Examiner
Art Unit **2191**
10/03/2005


TUAN DAM
SUPERVISORY PATENT EXAMINER